**CLEAN VERSION OF PENDING CLAIMS**

BURST/PIPELINED EDO MEMORY DEVICE
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*Claims 11-21 and 59-71 ,as of May 14, 2001 (Date of Response to First Office Action after RCE).*

11. A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected.

12. A storage device, as in Claim 11, wherein the storage device is asynchronous.

13. (Once Amended) A storage device, as in Claim 11, wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address to the switching circuitry.

14. A storage device, as in Claim 13, wherein the external address is temporarily stored in the temporary storage device prior to being sent to a decoder.

15. (Once Amended) A storage device, as in Claim 14, further comprising a counter coupled to the temporary storage device to receive a selected portion of the external address for generating an internal address.

16. (Once Amended) A storage device, as in Claim 15, wherein the internal address is provided to the temporary storage device through the switching circuitry.

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17. A storage device, as in Claim 16, wherein the patternless addressing scheme provides a pipelined extended data out pattern.

18. A storage device, as in Claim 17, wherein the patterned addressing scheme provides a burst extended data out pattern.

19. A storage device, as in Claim 18, wherein the switching circuitry includes at least one multiplexed device.

20. (Once Amended) A storage device, as in Claim 11, wherein the patternless addressing scheme is for a random column address access, and the patterned addressing scheme is for a sequential column address access.

21. (Once Amended) A storage device, as in Claim 20, wherein the sequence column address access is selected from a group consisting of an interleaved column address access and a linear column address access.

59. A memory device, comprising:

a memory array;

control logic operatively connected to the memory array, the control logic for selecting between an unpatterned pipeline and a patterned burst data pattern for accessing the memory array; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said pipeline scheme and said burst scheme is selected.

60. A memory device, comprising:

a memory array operable in a burst or a pipeline mode of operation;

control logic for selecting between the burst or the pipeline mode of operation; and

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switching circuitry for switching between a first, burst data pathway and a second, pipeline data pathway depending on which of the burst or pipeline modes of operation is selected.

61. A dynamic random access memory, comprising:

a plurality of addressable memory arrays;

a column address decoder for receiving an external column address;

control logic for selecting between a burst or a pipeline mode of operation based;

switching circuitry for switching between a burst pathway and a pipeline pathway depending on which of the burst or pipeline modes of operation is selected.

62. (New) A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme;

a counter; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected, wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address to the switching circuitry, and wherein the counter is coupled to the temporary storage device to receive a selected portion of the external address for generating an internal address.

63. (New) The storage device of Claim 62, wherein the internal address is provided to the temporary storage device through the switching circuitry

64. (New) The storage device of Claim 62, wherein the patternless addressing scheme provides a pipelined extended data out pattern.

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65. (New) A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected, wherein the patternless addressing scheme provides a pipelined extended data out pattern.

66. (New) The storage device of Claim 65, wherein the patterned addressing scheme provides a burst extended data out pattern.

67. (New) The storage device of Claim 65, wherein the switching circuitry includes at least one multiplexed device.

68. (New) A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected, wherein the patterned addressing scheme provides a burst extended data out pattern.

69. (New) The storage device of Claim 68, wherein the switching circuitry includes at least one multiplexed device.

70. (New) A memory device, comprising:

a memory array operable in a burst mode of operation or a pipelined mode of operation;

control logic for selecting between the burst mode of operation or the pipelined mode of operation; and

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switching circuitry for switching between a first, burst data pathway and a second, pipeline data pathway depending on which of the burst or pipelined modes of operation is selected, wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address to the switching circuitry.

71. (New) The memory device of Claim 70, further comprising a counter coupled to the temporary storage device to receive a selected portion of the external address for generating an internal address.

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